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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

NGUYEN, LINH V

ART UNIT

PAPER NUMBER

2819

DATE MAILED: 08/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/824,569	Applicant(s) KAPLAN, TODD	
	Examiner Linh V. Nguyen	Art Unit 2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 08 August 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) _____ is/are pending in the application.
4a) Of the above claim(s) 2-67 and 69 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 4-17, 20-33 and 48-67 is/are allowed.
- 6) ☒ Claim(s) 2, 3, 18, 19 and 41-47 is/are rejected.
- 7) ☒ Claim(s) 37-40 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

Response to Arguments

1. Applicant's arguments filed 8/8/05 with respect to improper of final rejection from previous office action e been fully considered. Therefore finality is withdrawing from the following non-office action

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 2, 3, 18, 19, and 34 - 36, are rejected under 35 U.S.C. 102(b) as being anticipated by Robertson et al. U.S. Patent No. 6,124,813.

Regarding claim 2, Fig. 5 and 7 of Robertson et al. disclose a switching arrangement comprising: a digital input comprising a first digital input portion (In A) and a second digital input portion (In B); a digital output (output of 20) comprising a first digital output portion (Out A) and second digital output portion (Out B); a switching element (20) between the digital input (A, B) and the digital output (Out A, Out B), the switching element having a first condition (No Swap) allowing the first digital output

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portion (Out A) to correspond to the first digital input portion (A) and the second digital output portion (Out B) to correspond to the second digital input portion (B), and a second condition (Swap) allowing the first digital output portion (Out A) to correspond to the second digital input portion (B) and the second digital output portion (Out B) to correspond to the first digital input portion (A) ; and a control arrangement (X1, X2, X3) to switch the switching element between the first condition and the second condition; a control arrangement (X1, X, X3) to switching (26) the switching element (20) between the first and second condition, wherein the control arrangement comprises analog processing elements (IN A, and IN B of the control arrangement X1, X2 are the output signals of analog processing elements of Flash Analog to Digital converter converter; See Fig. 14 [131]).

Regarding claim 3, wherein the control arrangement (X1 – X3) has a first control input (IN A) connected with the first digital input portion (A), a second control input (IN B) connected with the second digital input portion (B), and a control output (26), the control output (26) allowing the switching element to assume the second condition (Col. 5 lines 31 – 34) if the first digital input portion is different from the second digital input portion (Col. 4 lines 46 – 60).

Regarding claim 18, wherein the switching element is a multiplexer (Fig. 7[20] disclosing multiplexing system for transmitting multiple signals A and B; See Webster Dictionary for “multiplex”).

Regarding claim 19, wherein the switching element is a latched multiplexer (Fig. 7[20] disclosing multiplexing system for transmitting multiple signals by using switches

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24, 24 for engaging or latching the paths between input terminals [A, B] and output terminals [Out A, Out B]).

Regarding claim 34, Fig. 7 of Robertson et al. discloses a circuit comprising: a first input (A) and a second input (B); a control element (X1 – X3) connected with the first input and second input; a switch (20) either switching or not switching (Col. 4 lines 46 – 60) the first input (A) and the second input (B) according to the control element (X1 – X3); and a clocking (CLK) arrangement to pipeline (See Fig. 6 for disclosing multiples “pipelines” of the input digital signals) the first and the second input switch (IN A, IN B).

Regarding claim 35, wherein the first input (A) and the second input (B) are digital inputs (Col. 8 lines 5 – 6).

Regarding claim 36, wherein the control element comprises a delta-sigma modulator (Fig. 1).

4. Claims 41 – 47 are rejected under 35 U.S.C. 102(e) as being anticipated by Adams et al. U.S. 6,614,377

Regarding claim 41, Fig. 13 of Adams et al. discloses a digital-to-analog converter (232) mismatch shaper (150) comprising: a first input (Fig. 4 disclose a detailed circuit of scrambler circuit 150 having first input [IN A]) and a second input (Fig. 4 [IN B]); a control element (Fig. 4 [X1 – X3]) connected with the first input (IN A) and the second input (IN B); a switch (Fig. 4 [50]) either switching or not switching the first input and the second input according to the control element (Fig. 4[SELECT]); and a tuning arrangement (Fig. 13 [152]) to adjust a frequency spectrum of DAC errors, thus shaping the DAC errors away from a desired frequency band (See Fig. 14a – 14d).

Regarding claim 42, wherein the first input (Fig. 4 [IN A]) and the second input (Fig. 4 [IN B]) are digital inputs.

Regarding claim 43; wherein the control element comprises a delta-sigma modulator (Fig. 13).

Regarding claim 44, fig. 13 of Adams et al. further discloses wherein the delta-sigma modulator comprises a filtering element (212) and a quantizer (214).

Regarding claim 45, wherein the filtering element (212) comprises at least one delay element (210) every electrical device used to transfer signal is a delay element to its input signal).

Regarding claim 45, wherein the filtering element (212) comprises at least one delay element (every electrical device used to transfer signal is a delay element to its input signal).

Regarding claim 46, wherein the delay element comprises an adjustable gain circuit (the capacitor array is an adjustable gain circuit for the input signal. See Col. 1 lines 42 - 43).

Regarding claim 47, wherein the filter element (capacitor array) further comprises a plurality of transconductors (capacitor is an electrical conducting element used to transfer signal), and wherein the turning arrangement frequency (Fig. 13) adjusting at least one transconductor of the plurality of transconductors (Col. 1 lines 42 – 43 disclosing multiple transconductors capacitors having adjusting switches).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claim 69 rejected under 35 U.S.C. 103(a) as being unpatentable over Adams et al. U.S. patent No. 6,614,377, in view of Robinson et al. U.S. patent No. 6,873,280

Fig. 13 of Adams et al. discloses a mismatching noise shaping comprising: providing a circuit (150) the first circuit comprising: a first input (Fig. 4 (INPUT A) and a second input (Fig. 4 [IN B]), a control arrangement (Fig. 4 [X1 – X3]); and a switching arrangement either switching (Swap) or not switching (no swap) the first input and the second input according to the control arrangement (Fig. 4 [X1 – X3]); the circuit having a first circuit output (Fig. 4 [OUT A]) and a second circuit Output (Fig. 4 [OUT B]); providing a first DAC having a first DAC input and a first DAC output (Fig. 13 [232]); providing a second DAC having a second DAC input and a second DAC output (Fig. 13 [232]); connecting the first circuit output with the first DAC input and the second circuit output with the second DAC input (Fig. 13 [234]); summing the second DAC output from the first DAC output to provide a sum output; and inputting the sum output to a spectrum analyzer (Fig. 14A – 14E). However, Adams et al. teaches a summing DACs output instead of subtracting of DACs outputs.

Fig. 6 of Robinson et al. disclosing subtracting (232) a second DAC (226) from a first DAC (210) to provide a difference output (212) and output to a spectrum analyzer (Fig. 5)

Adams et al. and Robinson et al. are common subject matter of multiple DACs. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made the have utilizing the summing device 232 of Robinson et al. in to the summing device of Adams et al. for the purpose of monitoring the difference output among multiple DACs through the spectrum analyzer.

Allowable Subject Matter

7. Claims 37 - 40, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. With respect to claim 37, in addition to other elements in the claim, the prior art does not teach wherein the clocking arrangement clocks the filter element and the quantizer.

8. Claims 4 – 17, 20 - 33, 48 – 52, and 53 – 67, are allowed.

The following is an examiner's statement of reasons for allowance:

With respect to claim 4, in addition to other elements in the claim, the prior art does not teach wherein the control arrangement comprises a subtractor, subtracting the first digital input portion from the second digital input portion, the subtractor having a subtractor output with a first subtractor output value if the first digital input portion is not in a predetermined relationship with the second digital input portion and a second

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subtractor output value if the first digital input portion is in a predetermined relationship with the second digital input portion.

With respect to claims 48 and 53, in addition to other elements in the respective claim, the prior art does not teach a control element to control switching of the switch, the control element connected with the evaluation element and the switching element, the control element comprising a quantizer having a quantizer output, wherein switching between the first digital input and the second digital input depends on the quantizer output when the first digital input and the second digital input are in predetermined relationship therebetween and switching between the first digital input and the second digital input does not depend on the quantizer output when the first digital input and the second digital input are not in the predetermined relationship therebetween.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Contact Information

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (571) 272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Robert Pascal can be reached at (571) 272-1769. The fax phone

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numbers for the organization where this application or proceeding is assigned are
(571-273-8300) for regular communications and (571-273-8300) for After Final
communications.

08/15/05

Linh Van Nguyen

A handwritten signature in black ink, appearing to read 'Linh Van Nguyen', written in a cursive style.

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